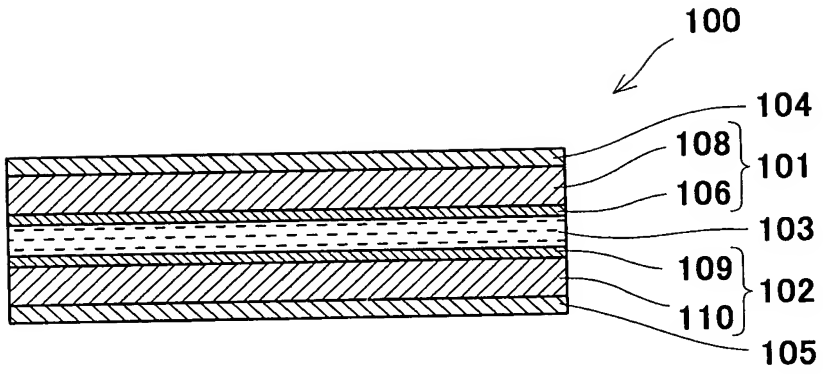

Fig. 1a

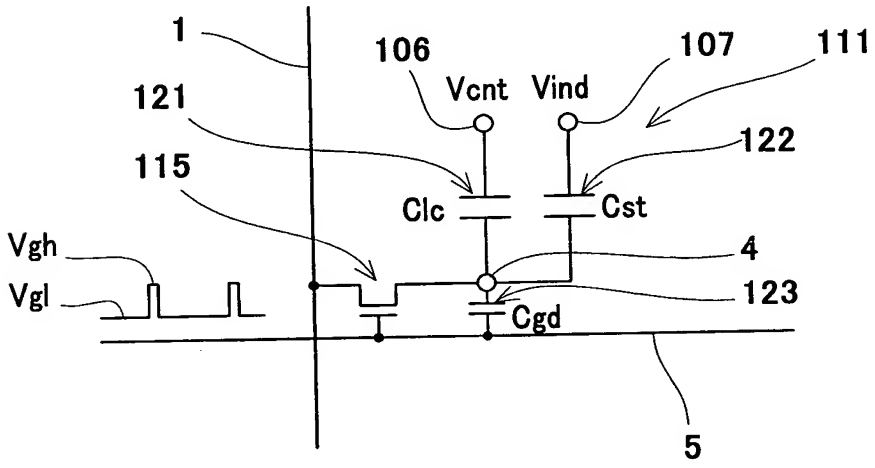

Fig. 1b

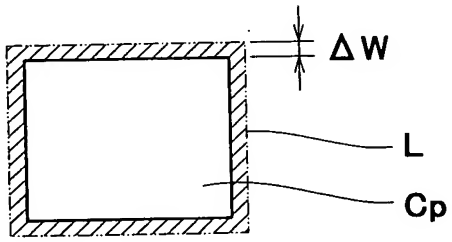

Fig. 2

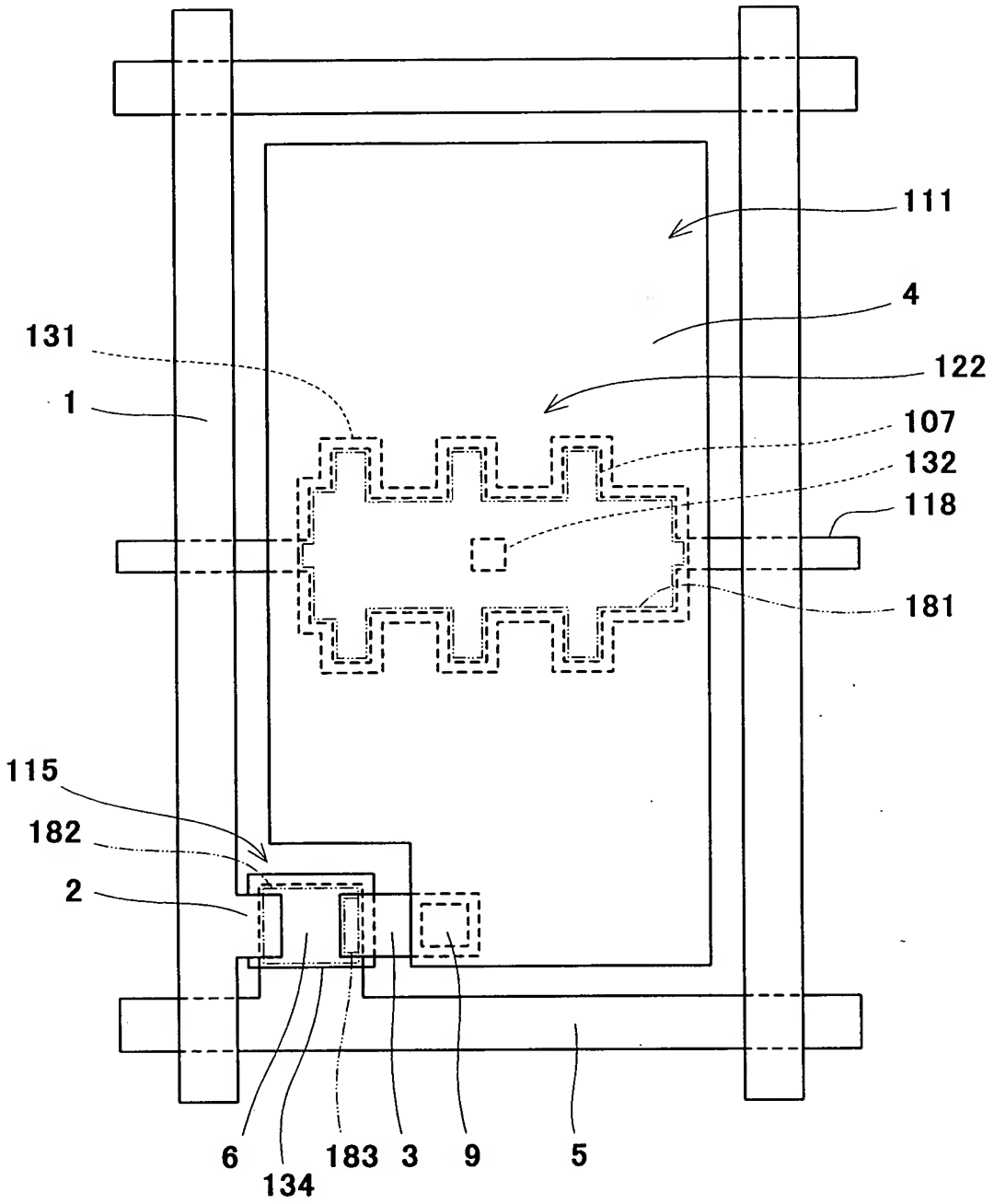

Fig. 3

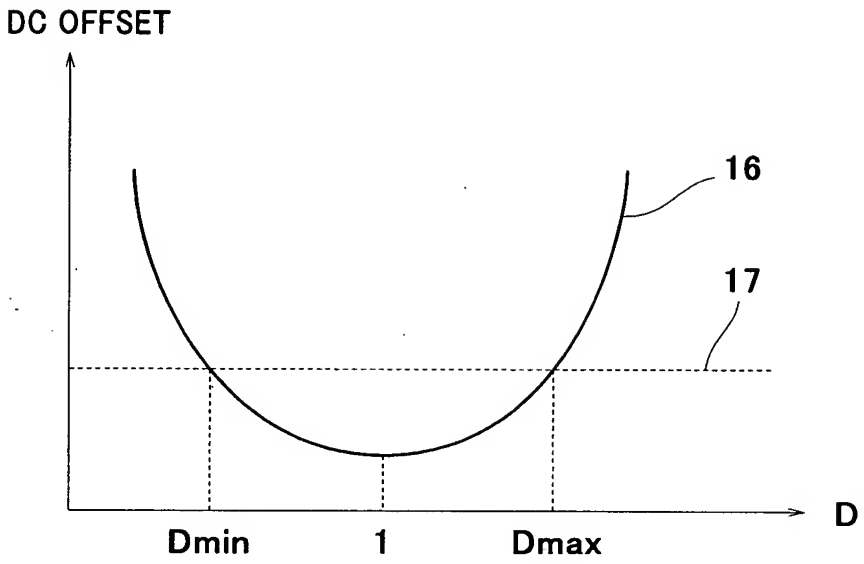

Fig. 4

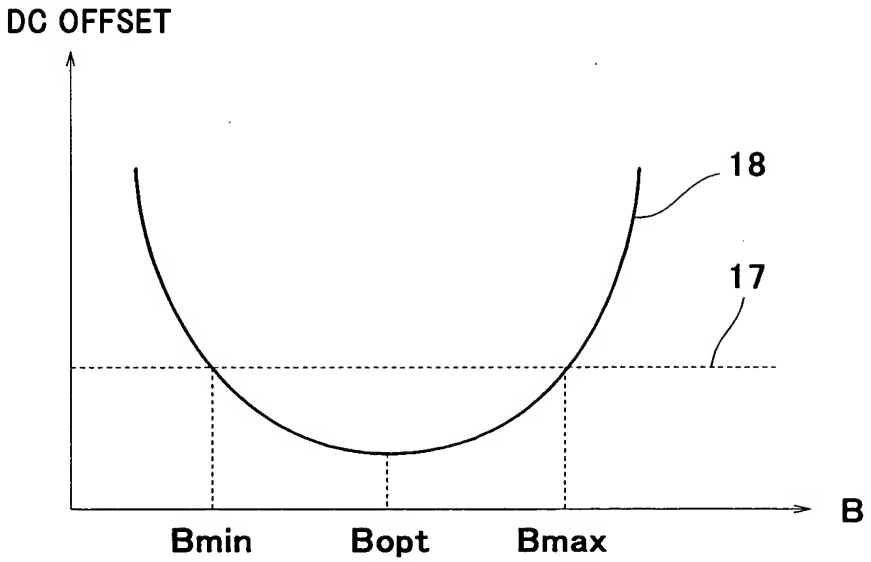

Fig. 5

Fig. 6a

Cst/Clc=0.5

	Cst(pF)	Lst(μm)	A	B	B'	D	Vts(V)	X
PRIOR ART	0.05	150	0.063	6.0	7.0	0.44	1.56	0.064
MINIMUM VALUE	0.05	282	0.063	11.3	12.3	0.77	1.56	0.064
OPTIMUM VALUE	0.05	375	0.063	15.0	16.0	1.00	1.56	0.000
MAXIMUM VALUE	0.05	481	0.063	19.2	20.2	1.27	1.56	0.064

Fig. 6b

Cst/Clc=1 (NORMAL VALUE)

	Cst(pF)	Lst(μm)	A	B	B'	D	Vts(V)	X
PRIOR ART	0.10	150	0.048	6.0	7.0	0.33	1.19	0.084
MINIMUM VALUE	0.10	342	0.048	13.7	14.7	0.70	1.19	0.084
OPTIMUM VALUE	0.10	500	0.048	20.0	21.0	1.00	1.19	0.000
MAXIMUM VALUE	0.10	687	0.048	27.5	28.5	1.36	1.19	0.084

Fig. 6c

Cst/Clc=1.5

	Cst(pF)	Lst(μm)	A	B	B'	D	Vts(V)	X
PRIOR ART	0.15	150	0.038	6.0	7.0	0.27	0.96	0.104
MINIMUM VALUE	0.15	387	0.038	15.5	16.5	0.63	0.96	0.104
OPTIMUM VALUE	0.15	625	0.038	25.0	26.0	1.00	0.96	0.000
MAXIMUM VALUE	0.15	918	0.038	36.7	37.7	1.45	0.96	0.104

Fig. 7a

CODE	VALUE	PARAMETER
Y(V)	0.1	DC OFFSET ALLOWABLE VALUE
Clc(pF)	0.1	LIQUID CRYSTAL CAPACITANCE
Cof(pF)	0.01	TFT GATE TO DRAIN CAPACITANCE VALUE
Lof(μm)	25	THE PERIPHERAL LENGTH OF THE PATTERN FORMING Cof
Sof(μm^2)	36	THE AREA OF THE PATTERN FORMING Cof
ΔW(μm)	0.5	DEVIATION OF THE WIDTHS OF PATTERNS WITHIN THE PANEL PLANE
ΔSof(μm^2)	12.5	DEVIATION OF THE AREA OF THE PATTERN FORMING Cof
E	0.347	{$=\Delta Sof/Sof$}
Vgh(V)	18	GATE ON VOLTAGE
Vgl(V)	-7	GATE ON VOLTAGE

Fig. 7b

Cst(pF)	VARIABLE VALUE	STORAGE CAPACITANCE VALUE
Lst(μm)	VARIABLE VALUE	THE PERIPHERAL LENGTH OF THE PATTERN FORMING Cst
A	VARIABLE VALUE	{$=Cof/(Clc+Cst+Cof)$}
B	VARIABLE VALUE	{$=Lst/Lof$}
B'	VARIABLE VALUE	{$=(Lst+Lof)Lof$}
D	VARIABLE VALUE	{$=A\times B'$}
Vts(V)	VARIABLE VALUE	{$=A\times(Vgh-Vgl)$}
X	VARIABLE VALUE	{$=Y/Vts$}
Dmin	VARIABLE VALUE	{$=(E-X)-(E\cdot(1+X))$}
D0	VARIABLE VALUE	{=1} (THE VALUE OF D WHEN X = 0)
Dmax	VARIABLE VALUE	{$=(E+X)-(E\cdot(1-X))$}

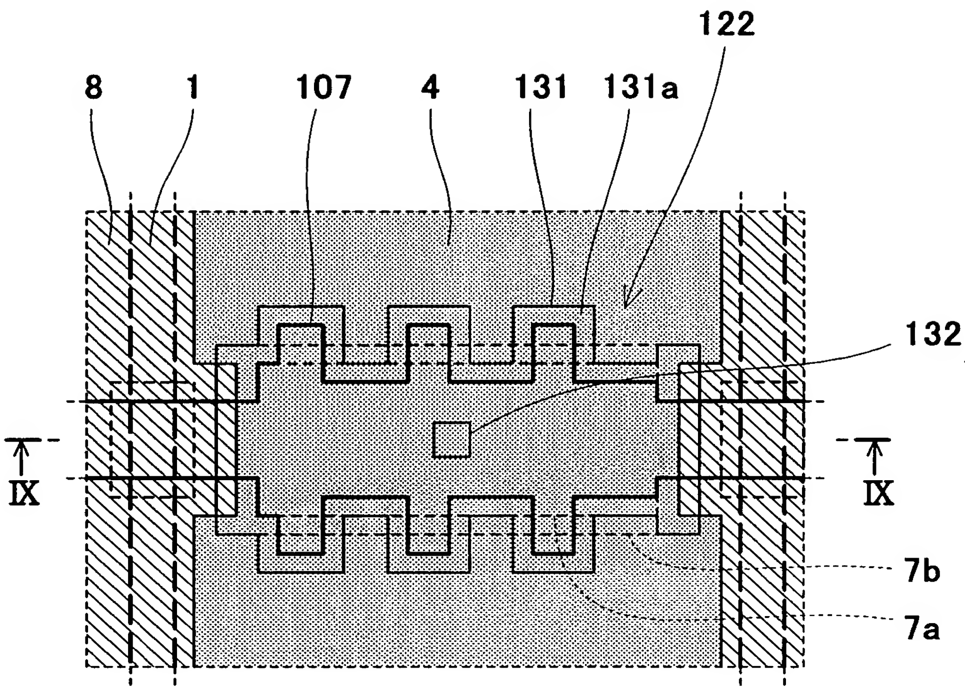

Fig. 8

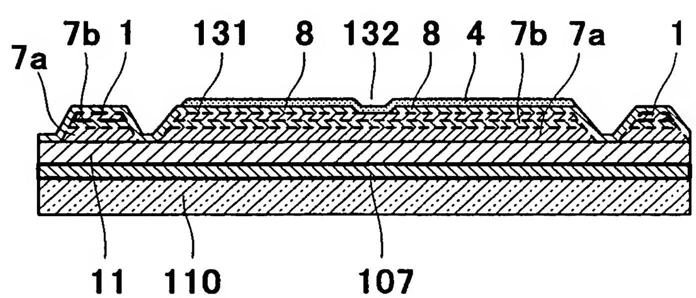

Fig. 9

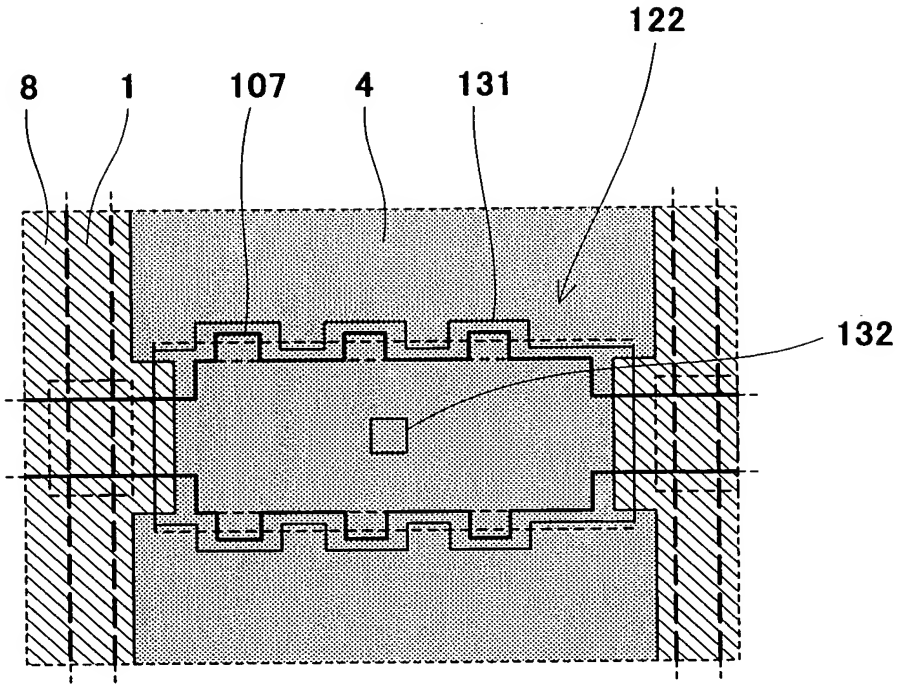

Fig. 10

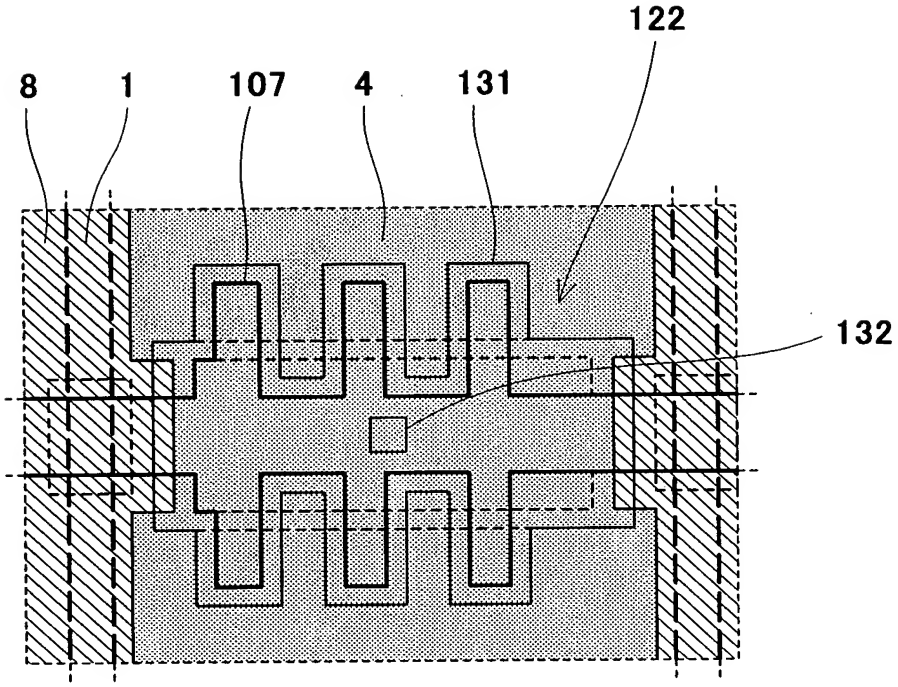

Fig. 11

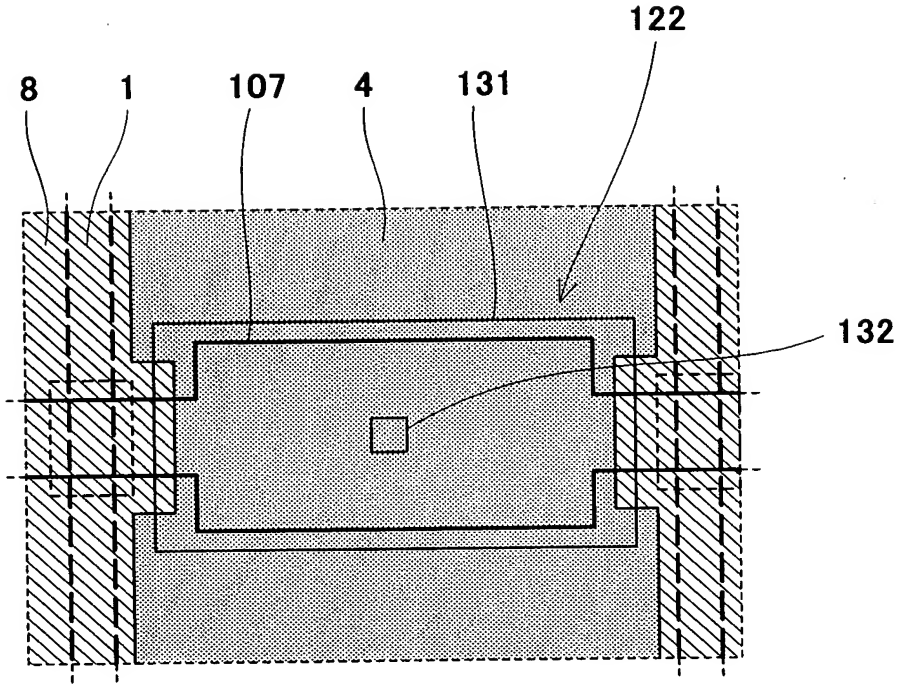

Fig. 12 PRIOR ART

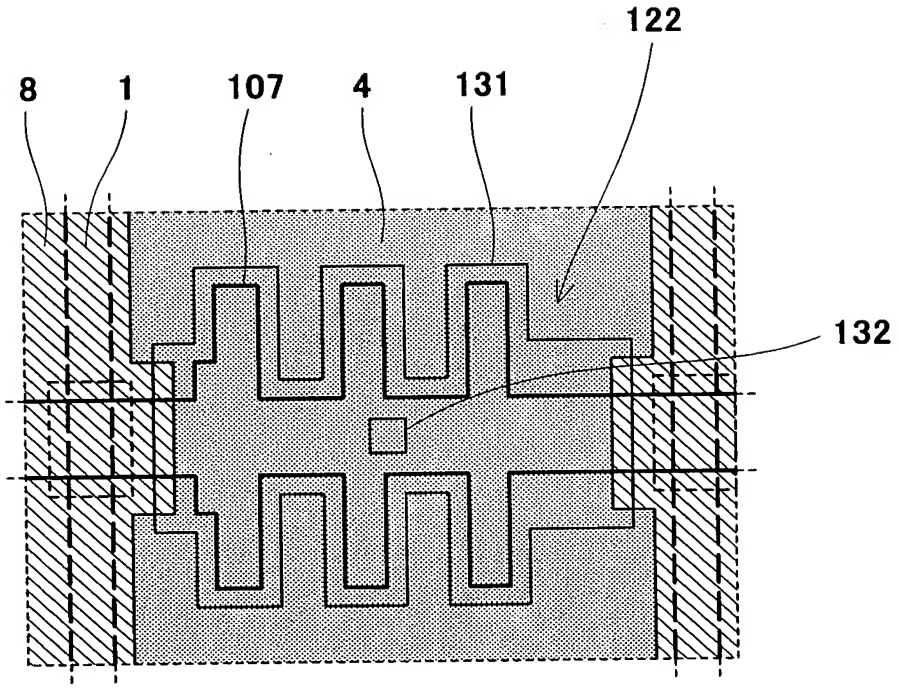

Fig. 13

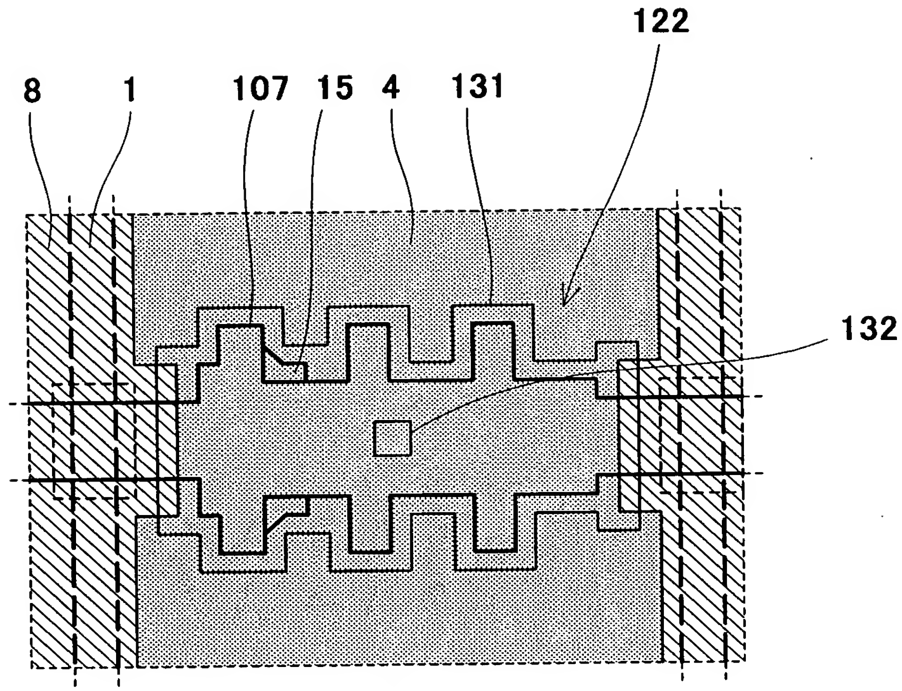

Fig. 14a

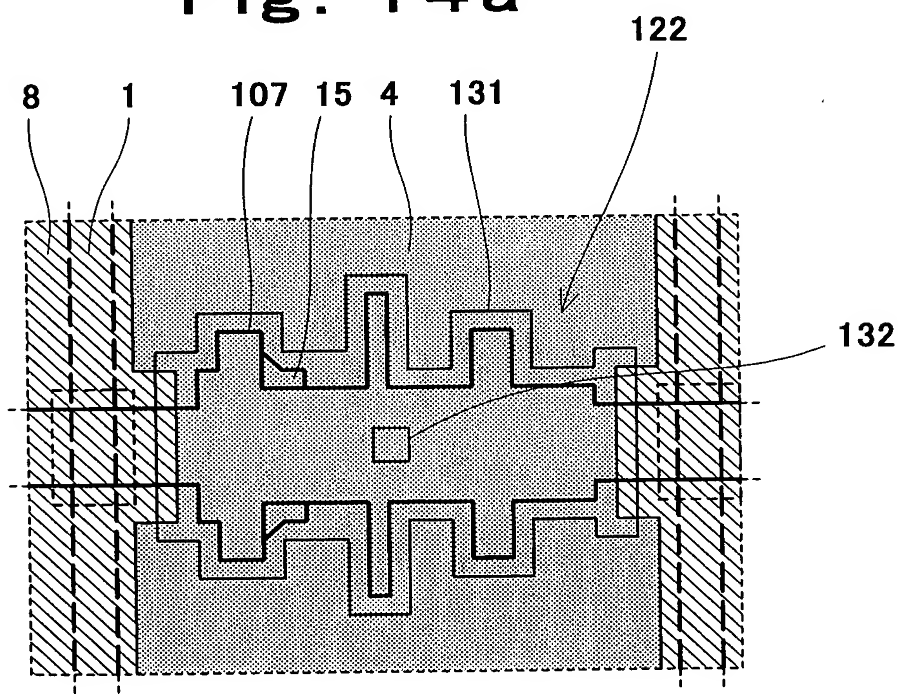

Fig. 14b

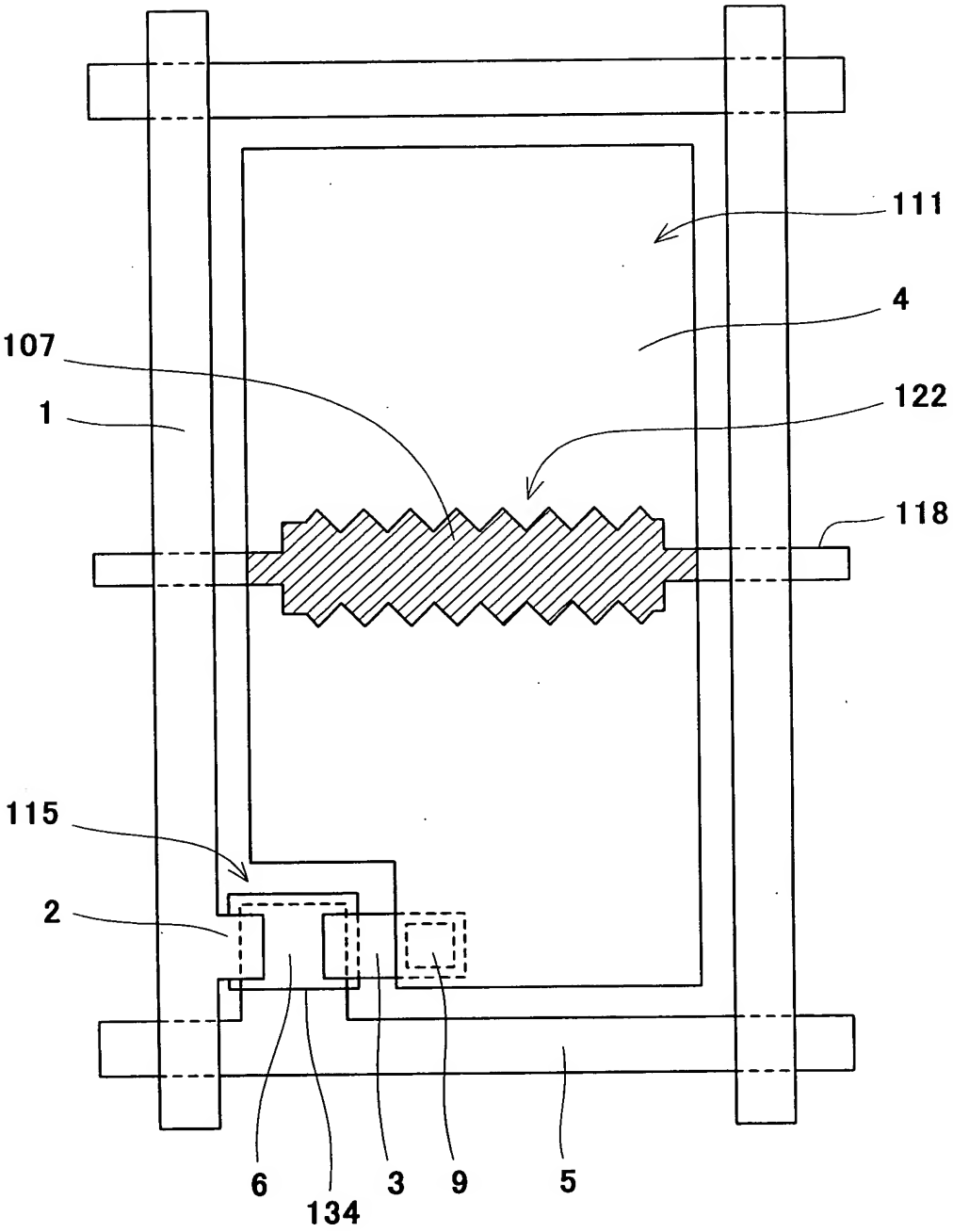

Fig. 15

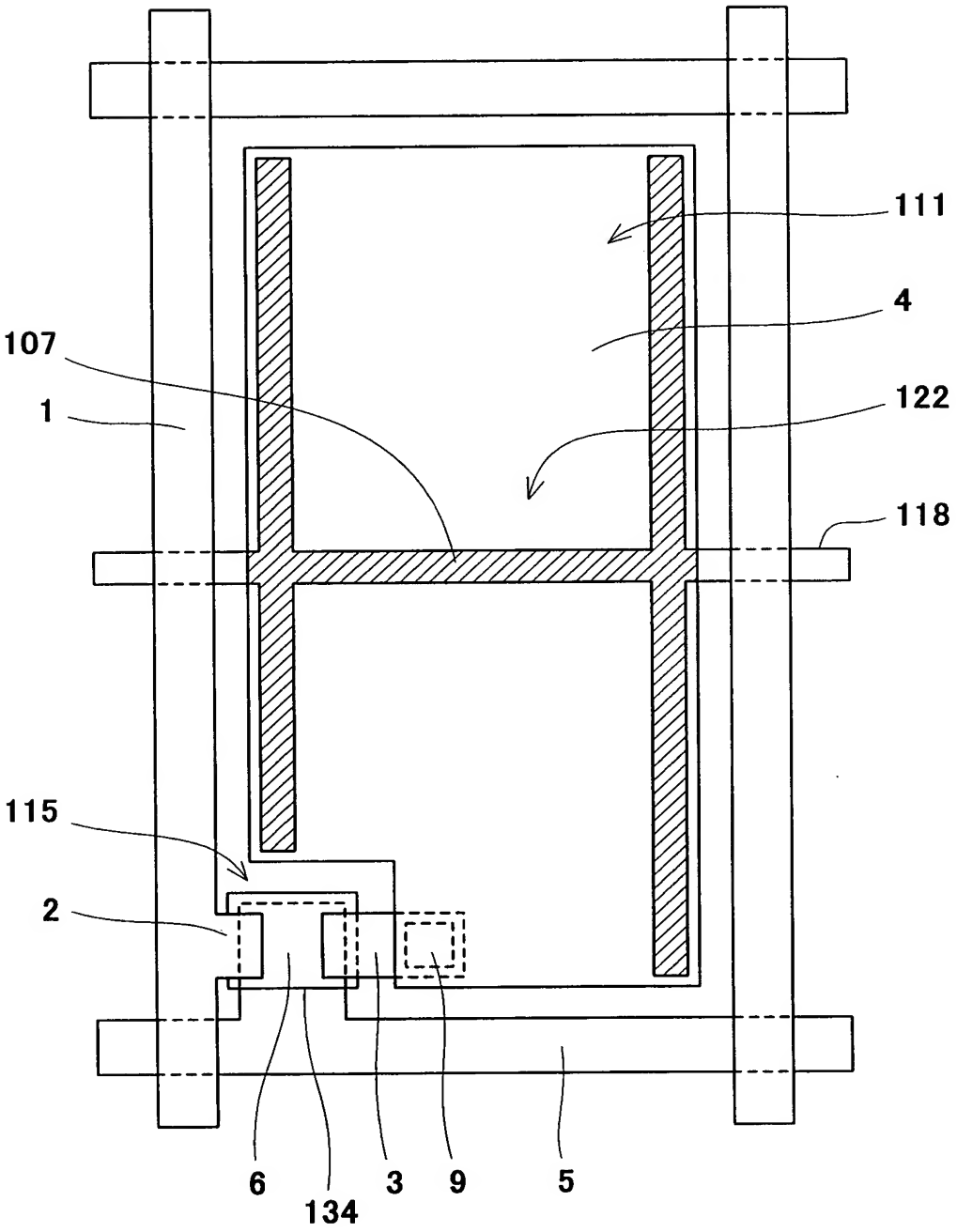

Fig. 16

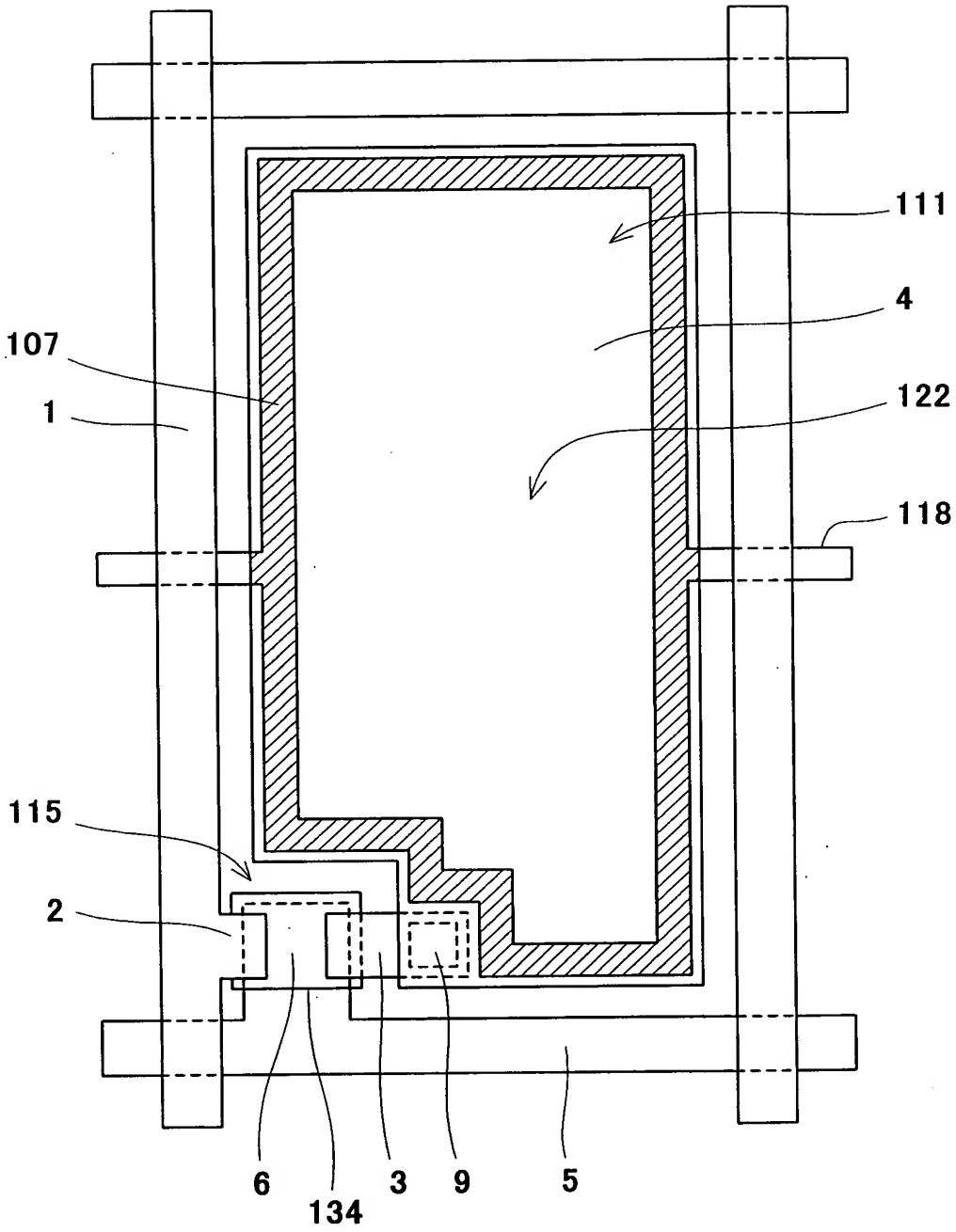

Fig. 17

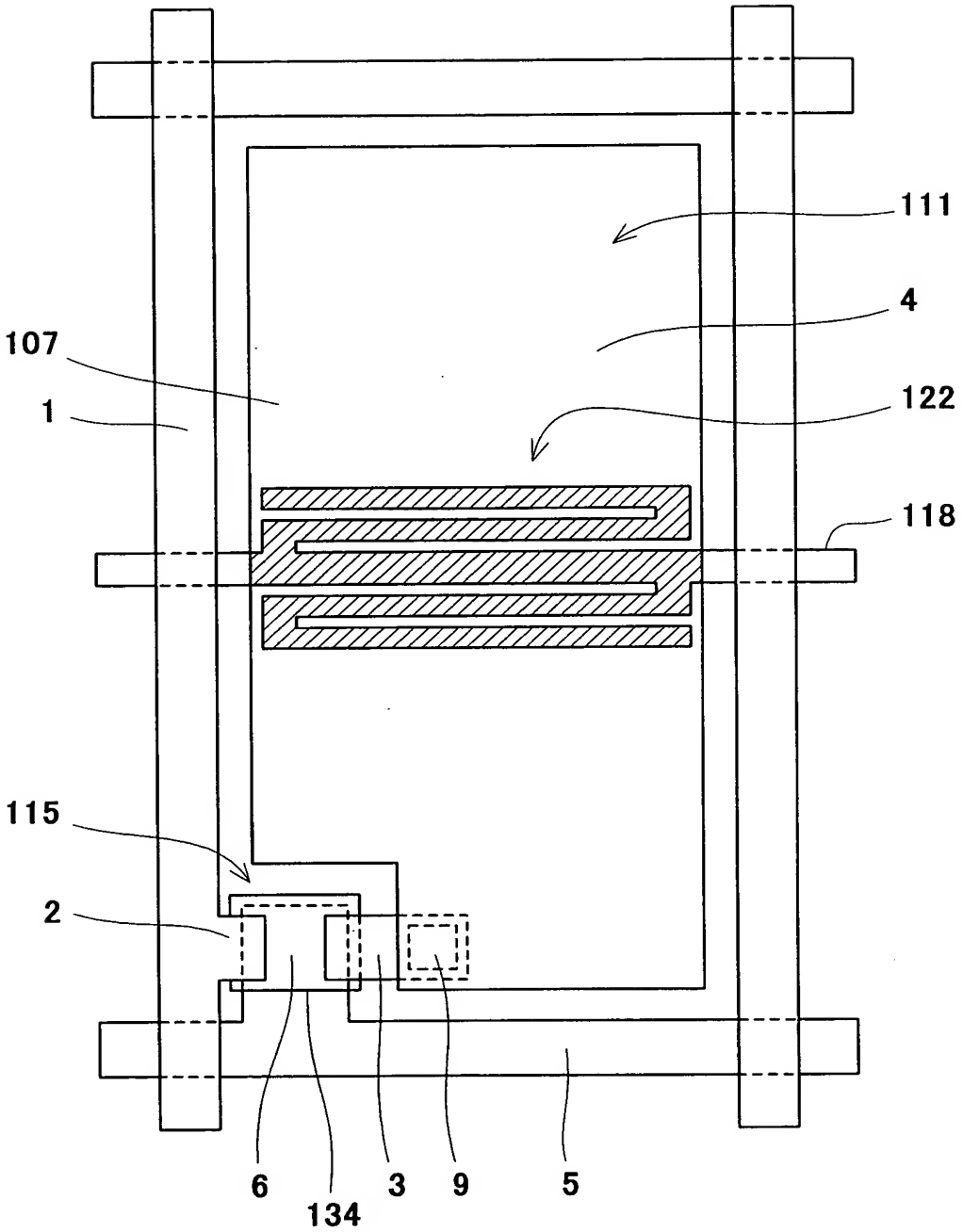

Fig. 18

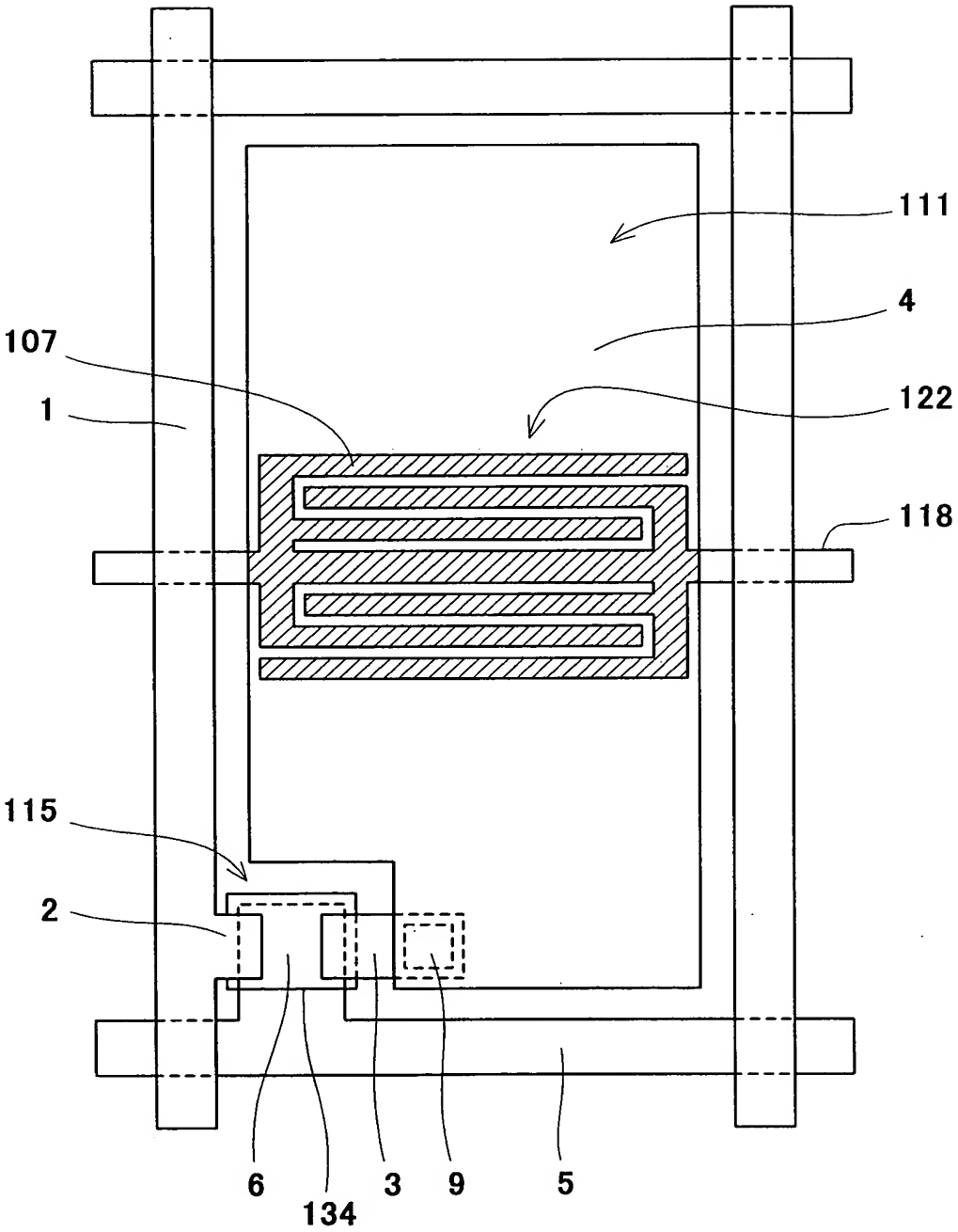

Fig. 19

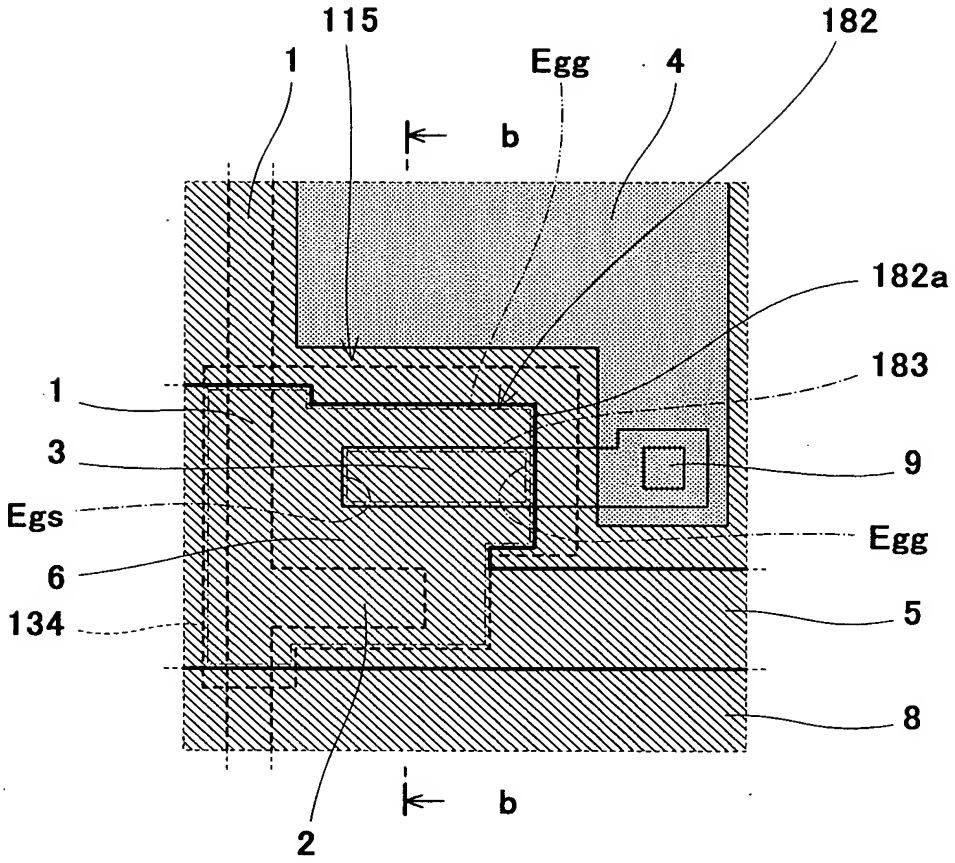

Fig. 21a

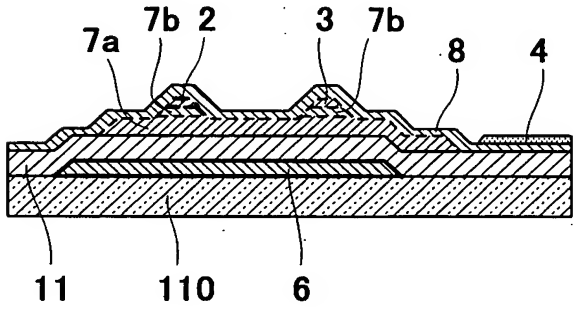

Fig. 21b

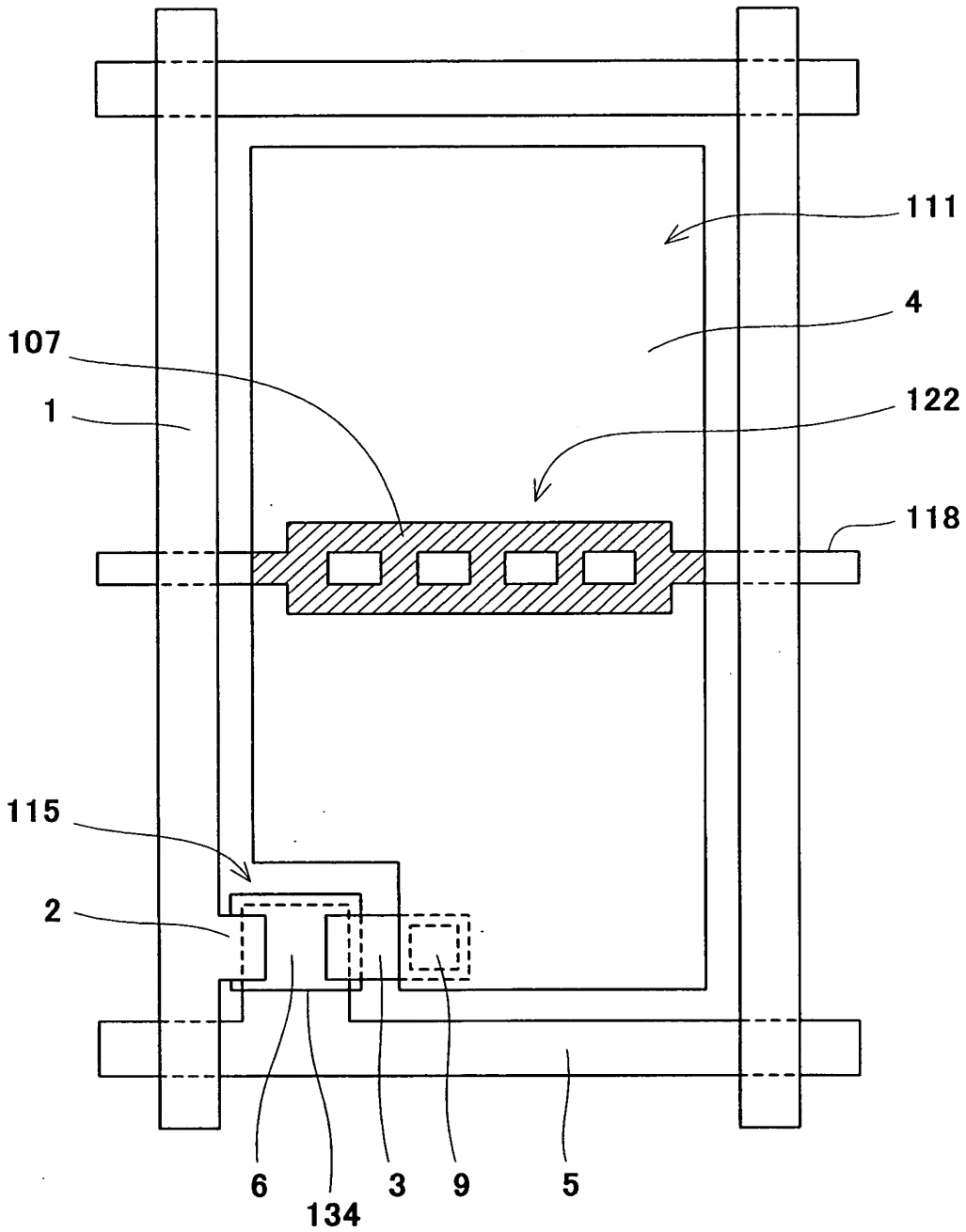

Fig. 20

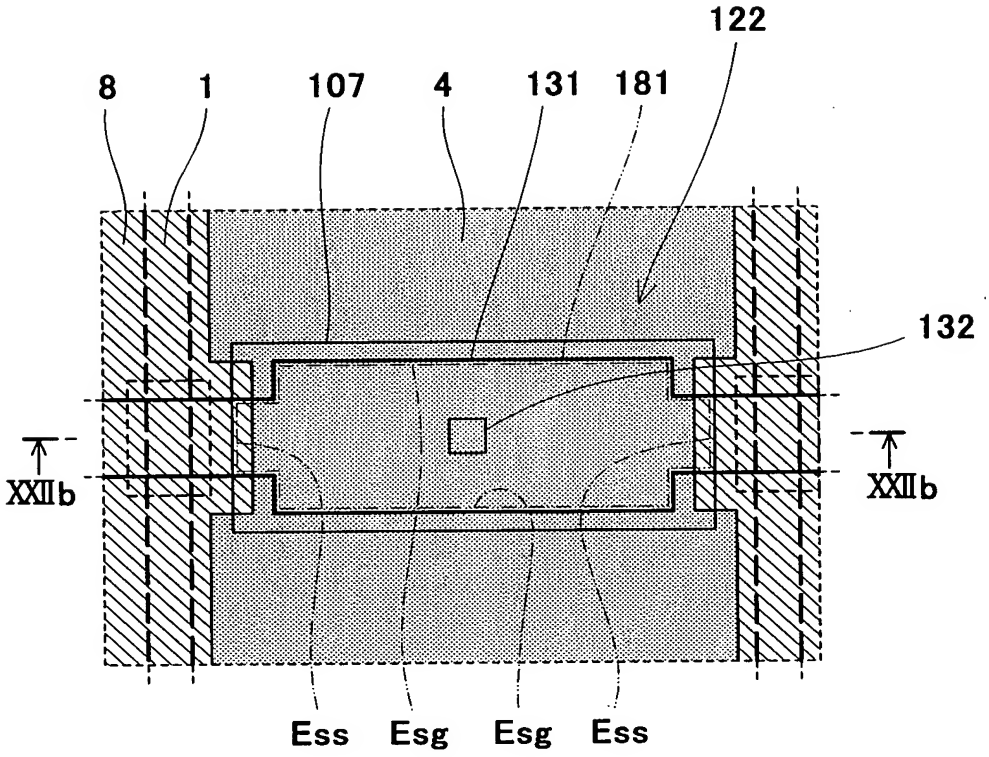

Fig. 22a

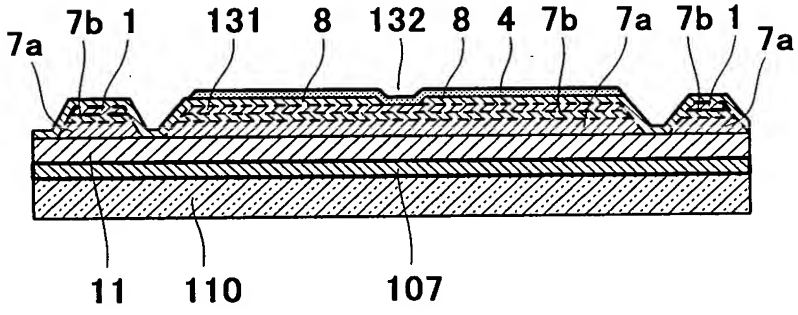

Fig. 22b

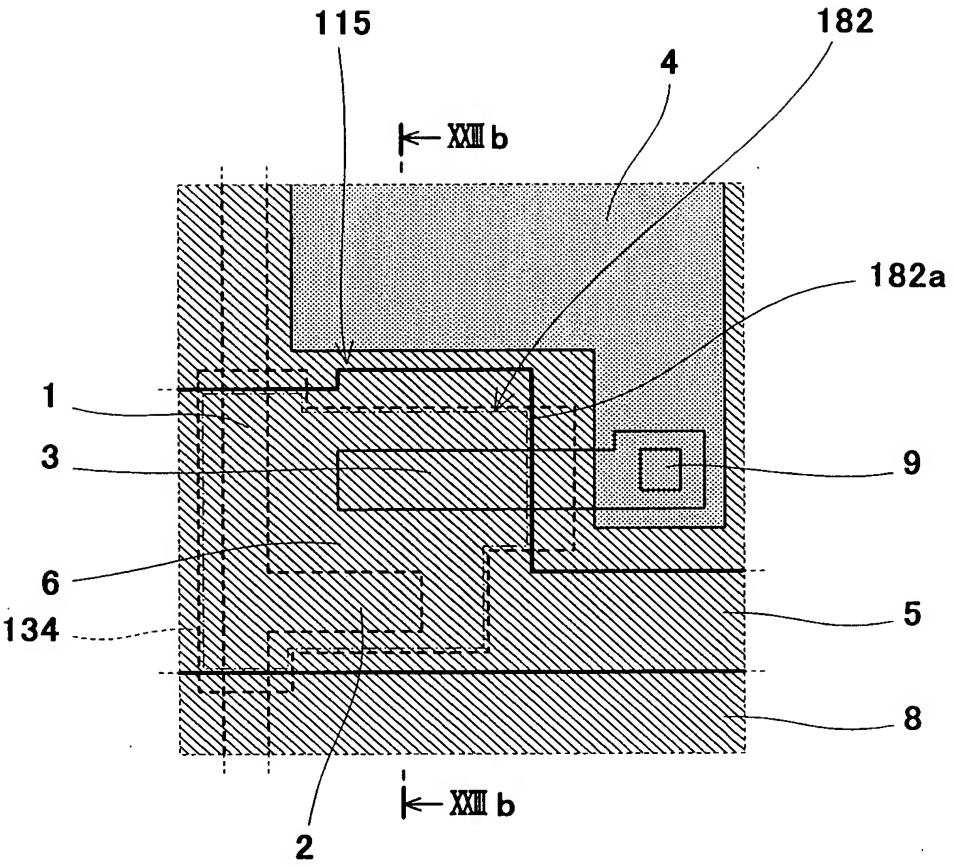

Fig. 23a PRIOR ART

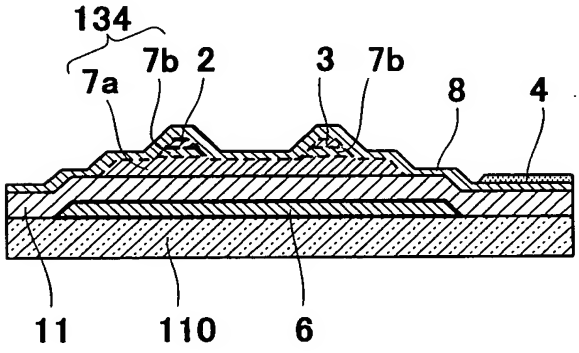

Fig. 23b PRIOR ART

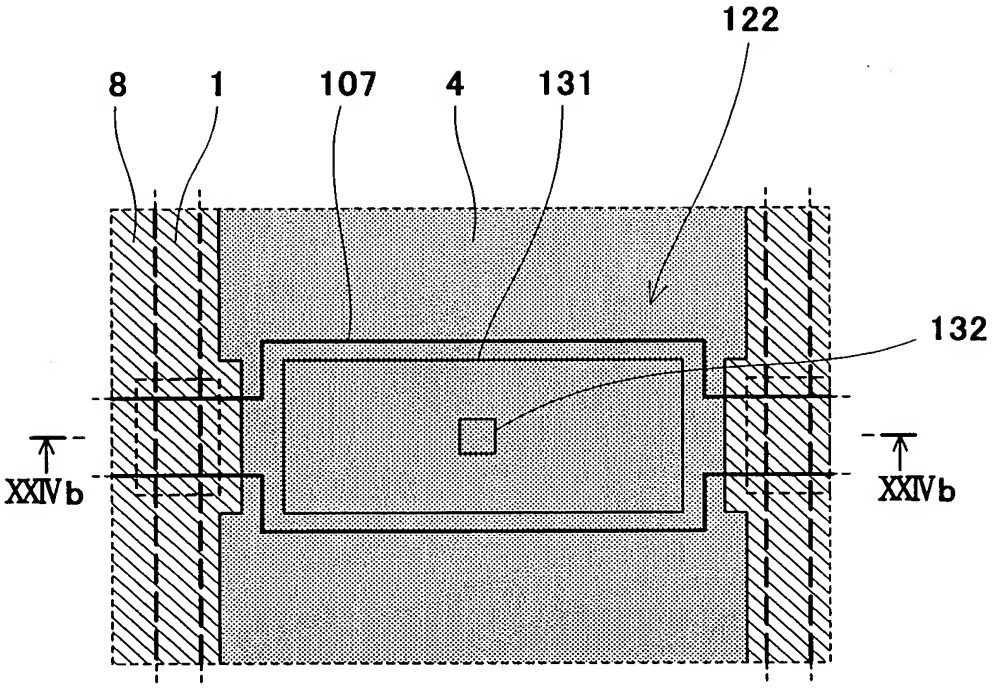

Fig. 24a PRIOR ART

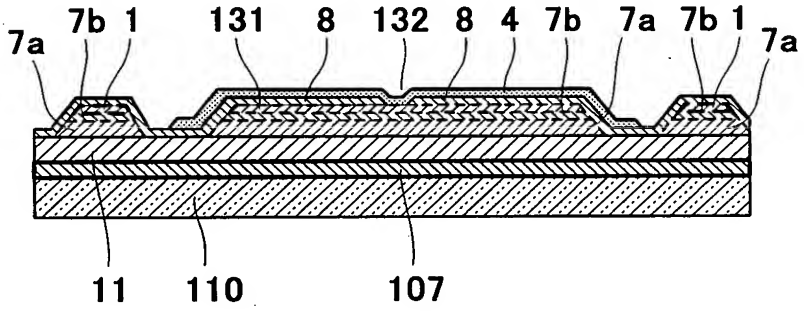

Fig. 24b PRIOR ART

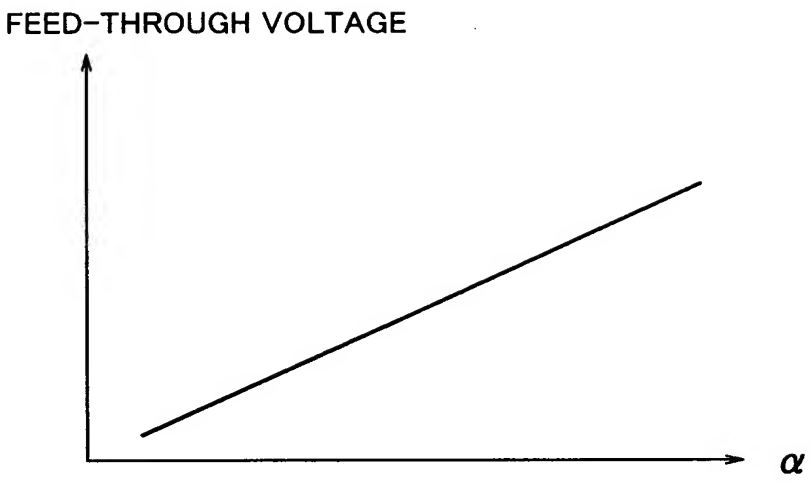

Fig. 25

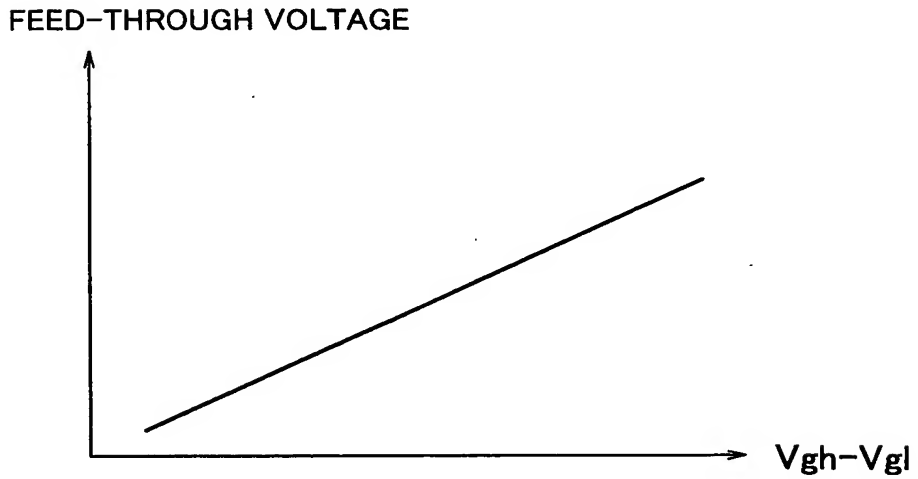

Fig. 26

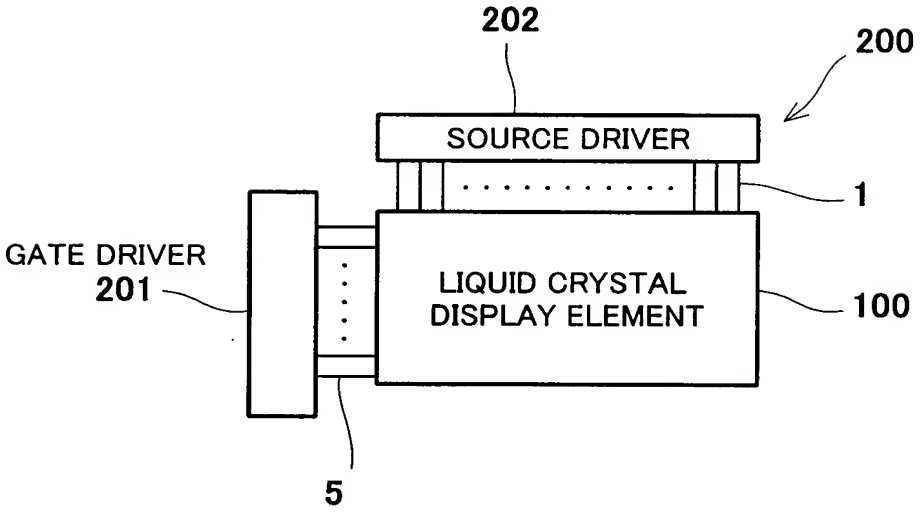
202
200
SOURCE DRIVER
1
GATE DRIVER
201
LIQUID CRYSTAL
DISPLAY ELEMENT
100
5

Fig. 27